REMARKS

This Amendment is filed in Response to the Office Action dated December 15, 2003; and as a Substitute for the Amendment filed on September 26, 2003; and in response to the Office Action dated June 27, 2003. All objections and rejections are respectfully traversed. All objections and rejections are respectfully traversed.

Claims 1-21, 28-36 and 38-53 are pending in the case.

Claims 1, 3, 7, 9, 10, 12, 13, 16-18, 19, 52, and 53 have been amended to better claim the invention.

Claim 37 has been cancelled without prejudice since it was nearly identical to pending claim 19.

Objection under 37 CFR §1.83(a)

At paragraph 2 of the Office Action the drawings were objected to under 37 CFR §1.83(a) as not showing every feature of the invention specified in the claims. Examiner stated the "micro-opcodes to initiate memory prefetches without requiring a dedicated instruction" as claimed in claim 45 were not shown in the drawings.

Applicant would like to direct the Examiner's attention to the box labeled 506 in Fig. 5 of the drawings. As the text at page 10, lines 23-24 of the specification describes, box 506 depicts "a 10 bit C part 506 comprising three micro-opcode fields." Applicant respectfully requests the objection to the drawings be withdrawn in light of box 506 of Fig. 5.

Rejections under 35 USC §112, first paragraph

At paragraphs 5-6 of the Office Action claim 45 was rejected under 35 USC §112, first paragraph as containing subject matter not described in the specification in such a way as to convey to one skilled in the art that the inventor(s) had possession of the claimed invention. Examiner stated the claimed "micro-opcodes to initiate memory prefetches without requiring a dedicated instruction" were not described in the specification.

Applicant would like to direct the Examiner's attention to page 10 of the specification, which repeatedly describes the micro-opcodes used in the invention. Lines 12-13 of page 10 teach "each instruction word contains two major opcodes and up to three minor opcodes (micro-ops) that execute in parallel." Lines 15-17 of page 10 teach the "instruction set architecture provides mico-opcodes to initiate memory prefetches without requiring a dedicated instruction." Finally, lines 23-24 of page 10, in reference to Fig 5, describe a "10-bit C part 506 comprising three micro-opcode fields." Applicant respectfully requests that, in light of the repeated description of the micro-opcodes, the rejection to claim 45 under 35 USC §112 be withdrawn.

At paragraph 7 of the Office Action claim 45 was rejected under 35 USC §112, first paragraph as containing subject matter not described in the specification in such a way as to be enabling.

In light of the repeated description of the opcodes on page 10 of the specification and in Fig. 5 of the drawings, as detailed above, Applicant respectfully requests this rejection also be withdrawn

Objection under 37 CFR 1.75(d)(1) and MPEP § 608.01(o)

At paragraphs 8 of the Office Action claim 45 was objected to under 37 CFR 1.75(d)(1) and MPEP § 606.01(o) as failing to provide proper antecedent basis for claimed subject matter. Examiner asserts "micro-opcodes to initiate memory prefetches without requiring a dedicated instruction" does not exist within the specification.

Applicant would like to direct the Examiner's attention to page 10, lines 15-17 of the specification which state "mico-opcodes to initiate memory prefetches without requiring a dedicated instruction." Since the language in the specification is identical to the language used in claim 45, Applicant respectfully requests the antecedent basis objection be withdrawn.

Rejections under 35 USC §112, second paragraph

At paragraph 9 of the Office Action claim 46-51 were rejected under 35 USC §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter of which Applicant regards as the invention. Examiner specifically directs the rejection to the words "one of" in claim 46.

Applicant believes "one of" was a typographical error and in accord with the Examiners suggestion, has deleted the words from claim 46. Therefore, Applicant respectfully requests the rejection under 35 USC §112, second paragraph be withdrawn.

Rejections under 35 USC §102

At paragraph 13 and 14 of the Office Action Claims 1-21, 36-37 and 52-53 were rejected under 35 USC §102 as being unpatentable in view of Asato, U.S. Patent No. 6,578,086 issued on November 7th, 2000 (hereinafter Asato).

The present invention, as set forth in representative claim 1 comprises:

1. Apparatus for enabling an instruction to control data flow bypassing hardware within a processor of a programmable processing engine, the apparatus comprising:

a pipeline of the processor, the pipeline having a plurality of stages including instruction decode, writeback, and execution stages, the execution stage having a plurality of parallel execution units; and

an instruction set of the processor, the ***instruction set defining a first register decode value that defines source operand bypassing that allows source operand data to be shared among the plurality of execution units***, and a second register decode value that defines result bypassing that allows bypassing of a result from a previous instruction executing in pipeline stages of the processor.

The Asato patent describes a system with result bypassing where a selector bypasses the result of a proceeding instruction to be used as a source operand of a subsequent instruction (Col. 5, lines 57-62). A "bypass information specification field" of an instruction directs the operation of the source operand selector (Col. 5, lines 21-29). Despite Asato's references to a misleadingly named "source operand bypass specification field" in the abstract, Asato only describe a scheme for result bypassing.

Applicant respectfully urges that Asato does not show Applicant's claimed invention relating to an "***instruction set defining a first register decode value that defines source operand bypassing that allows source operand data to be shared among the plurality of execution units.***" In response to Examiner's previous comment, Applicant has amended claims 1, 9, and 19 to remove the words "one of." Apparently Examiner interpreted "one of" as alternative claiming language. Applicant has amended the claims to clarify that alternative claiming language was not intended.

Briefly discussed, Applicants' invention allows bypassing of either an operation result or a ***source operand*** of a parallel execution unit. To take example from page 14 of the specification:

(i5) M add R1 ← R2, 5(R3)

(i6) S and R2 ← RISB, R3

In the example, the processor has two parallel units, the M-Unit and the S-Unit. In the above instruction, the M-Unit executes the M add instruction, fetching the displacement operand 5(R3) over the local bus 424. (Application pg. 14; Application Fig. 6). Although the S-Unit has no direct connection to the local bus, the RISB operand in instruction **i6** indicates that the data fetched in the M-Unit from the local bus will be shared with the parallel S-Unit as a source operand through the parallel connection via the multiplexer. The S-Unit lacks direct access to the local bus because encoding a displacement operand requires more bits than possessed by the S-Unit instruction field. (Application pg. 10). Source bypassing enables the parallel S-Unit to use the data transferred over the local bus, while still using fewer bits in the instruction field.

The Asato patent makes absolutely no mention of source operand bypassing. Indeed, Asato only describes a scheme for result bypassing. Asato's "source operand bypass specification field" is simply a field to control result bypassing.

Therefore, Applicants respectfully urge that the Asato patent is legally precluded from anticipating the claimed invention under 35 U.S.C. §102 because of the absence from the Asato patent of Applicants' "***instruction set defining a first register decode value that defines source operand bypassing that allows source operand data to be shared among the plurality of execution units***

Rejections under 35 USC §103

At paragraph 19 of the Office Action claims 28-35, 40-51, an 42-53 were rejected under 35 USC §103 as being unpatentable over Nakada, U.S Patent No. 5,638,526 issued on Jun 10th, 1997 (hereinafter Nakada) in view of Asato, U.S. Patent No. 6,578,086 issued on November 7th, 2000 (hereinafter Asato).

The present invention, as set forth in representative claim 28 comprises:

28. A processor comprising:
a first execution unit having at least one first input and a first output;
at least one second execution unit having at least one second input and a second output;
a first input register connected to said at least one first input;
a second input register;
a multiplexer having a first input from said first input register, a second input from said second input register, and an output to said at least one second execution unit; and
a register decode value that specifies bypassing data from said first input register to said at least one second execution unit via said multiplexer.

The Nakada patent describes a system for a form of operand bypassing. In the Nakada system, a comparator circuit detects coincidence between data in a cache register for the current instruction and the operand of the next instruction (Col. 4, lines 17-21). The comparator then causes a selector to move the data in the cache register back to the same, or a different, cache register to be used with the next instruction (Col. 4, lines 11-15, 21-26, and see Fig. 4). Since the operand is moved from one cache register to another cache register (or in some cases the same cache register) the operand will only be available at a later clock cycle, adding delay to the system (See Fig 4).

Applicant respectfully urges that neither Nakada, Asato, nor any combination thereof shows Applicant's claimed invention relating to "***a multiplexer having a first input from said first input register, a second input from said second input register, and an output to said at least one second execution unit.***" Asato makes absolutely no mention of operand bypassing. Nakada teaches a different type of operand bypassing than the claimed invention. Nakada teaches bypassing from a cache register (Fig 4, item OP11) to a second cache register (Fig 4, items OP11, OP12, OP21, OP22). One skilled in the art would see from Fig. 4 that an operand bypassed in this manner would only be available at a later clock cycle. This is an undesirable result.

Dissimilarly, Applicant claims operand bypassing from a cache register directly to an ALU, without an intervening register and the associated delay problems of this type of implementation. In brief, Applicants invention bypasses the contents of interstage register M-ISR1A (Application Fig, 6, item 646) via a multiplexor (Application Fig 6., item 658) directly to the S-ALU (Application Fig. 6, item 656). The operand is <u>not</u> passed back to a register. Therefore, Applicants respectfully urge that neither Nakada, Asato, nor any combination thereof anticipate the claimed invention under 35 U.S.C. § 103 because of the absence in either patent of "***a multiplexer having a first input from said first input register, a second input from said second input register, and an output to said at least one second execution unit.***"

All independent claims are now believed to be in condition for allowance.

All dependant claims are believed to be dependant from allowable independent claims.

Applicant respectfully solicits favorable action.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

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